STACKED FIP-CHIP PACKAGE

ABSTRACT

A stacked flipchip package is disclosed comprising two chip carriers, each of which includes at least a chip and a plurality of solder bumps formed on the active surface of the chip used to electrically connect the chip to the chip carrier. A first chip carrier is joined "back to back" with a second chip carrier via an insulating adhesive applied on the inactive surface of the first chip mounted on the first chip carrier and the inactive surface of the second chip mounted on the second chip carrier. Wherein the two inactive surfaces are bonded together to form a multichip module. Both the topmost surface and the lowermost surface of the multichip module are capable of being electrically connected with other components, thereby eliminating one of the obstacles associated with vertically stacking chips in flip-chip technology and further varying arrangement flexibility of the chips in a package.